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A study of current –voltage characteristics of ITO/(p)Si heterojunctions

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Abstract : A ITO/(p)Si heterojunction was fabricated by depositing Indium Tin Oxide (ITO) thin films onto well cleaned p-type silicon wafer by thermal evaporation method from pure ITO powder at substrate temperature 523K. The different diode parameters were calculated from the current-voltage characteristics of the junctions. The diode ideality factor was found to be greater than 1 and the diode had high series resistance. The I-V characteristics under illumination showed poor photovoltaic effect of the junction. Large series resistance, high defect density and presence of interfacial layer are thought to be the main causes for higher value diode ideality factor and poor photovoltaic conversion efficiency.

Keywords : Indium Tin Oxide, thermal evaporation, diode ideality factor, photovoltaic effect

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1. Introduction

Indium Tin Oxide (ITO) is a degenerate semiconductor having band gap of approximately 3.6 eV. This high conducting material with high transparency in visible region is a good transparent electrical conductor. ITO has been used as a transparent electrode in advanced optoelectronic devices such as solar cells, light emitting and photo diodes, photo transistors and liquid crystal displays. Thin films of Indium Tin Oxide have been reported to be prepared by variety of techniques such as spray pyrolysis, sputtering, reactive evaporation, pulsed laser deposition, thermal evaporation method *etc* [1-7]. The property of a film depends on the method of preparation. Studies of ITO-Si structures have been reported by some workers where the ITO films were deposited by *rf* sputtering [3] or spray pyrolysis method [1, 2]. However, not much information have been obtained for junctions of ITO film

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prepared by thermal evaporation directly onto the Si substrate. The evaluation of diode parameters provides a useful guidance for further characterizing this device structure. In the present investigation, ITO films were deposited by thermal evaporation method from ITO powder on silicon wafer to form ITO/(p)Si heterojunction and their current-voltage (*J-V*) characteristics were studied. Different electrical parameters of the junction calculated from these characteristics have been presented in this paper.

2. Experimental

The ITO thin films of thickness about 2000 Å were prepared by thermal evaporation of pure Indium Tin Oxide powder (99.999%) in a vacuum better than 10^{-5} Torr, at a deposition rate of about 1Å /sec. ITO films were vacuum deposited on chemically cleaned glass substrates for studying their electrical and optical properties. During deposition the substrates were kept at a temperature of 523K. For the preparation of a heterojunction, initially, Al electrodes were vacuum deposited on one side of (p)Si wafers to make ohmic contacts and then ITO films were deposited on the other side, thus making ITO/(p)Si-Al structures. The specifications of Si wafers used were: boron-doped (p-type), orientation (100), resistivity 10-20 ohm cm, thickness 50000-55000 Å and area 1.5x1.5 cm^2. Before deposition of counterelectrodes for measurement, ITO films as well as the junction structures were annealed for one hour at 350K temperature. This was done in order to improve the conductivity and transparency of the ITO films as reported in our earlier study [7]. Countertoelectrodes of Al were vacuum deposited over ITO films for making ohmic contacts to ITO films. Thus structures of the type Al-ITO/(p)Si-Al were obtained. For electrical study of ITO film, a gap type structure was formed by depositing Al electrodes on two ends of the thin films keeping a gap between them. The conductivity was measured from I-V characteristics of the ITO film. The thickness of the films was measured by multiple interference method [8]. The optical transmittance was studied with the help of a UV-visible spectrophotometer (Cary 300, Varian, Australia). For all current-voltage and photovoltaic measurements, the junctions were mounted on a sample holder kept inside a specially designed metal chamber evacuated up to 10^{-2} Torr using a rotary pump. For current measurement an Electrometer (Keithley model 6514, USA) was used. For J-V measurement under illumination, the junction in the chamber was illuminated through a glass window using white light from a tungsten-halogen lamp. The details of experimental arrangement has been reported elsewhere [9, 10]. The C-V measurements were performed on the junctions at room temperature, using a digital Autocompute LCR-Q (Aplab-4910) meter.

3. Results and discussion

The electrical conductivity of the prepared ITO films was found around $1.5\text{x}10^{-2}$ $\Omega^{-1}cm^{-1}$ with sheet resistivity of 3375 KΩ/square. The optical transmittance of a typical ITO film in the wavelength from 300nm to 600nm after annealing is shown in Figure 1. From Figure, it is seen that the optical transmittance of the film is about 74% at wave length of 550nm.

The J-V characteristics of a few typical ITO/(p)Si junctions in dark have been shown in Figure 2. The curves exhibited rectifying nature of a Schottky diode in the forward direction. Under the forward bias the current increases exponentially with voltage. In reverse bias

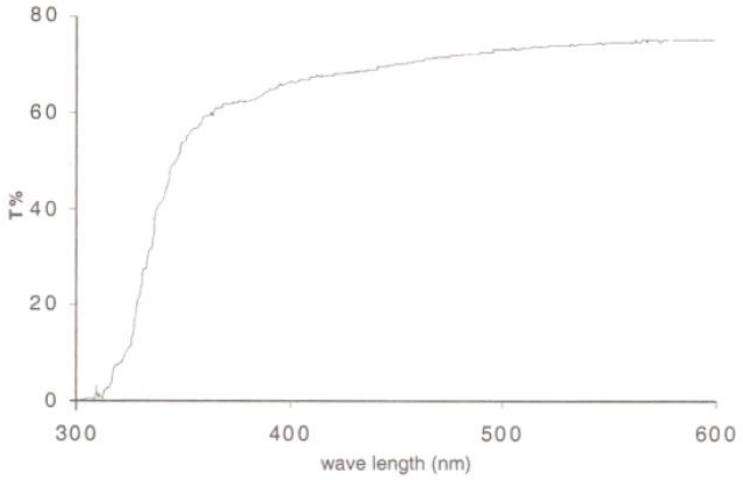

Figure 1. Transmittance *vs* wavelength of ITO films of thickness 2000Å.

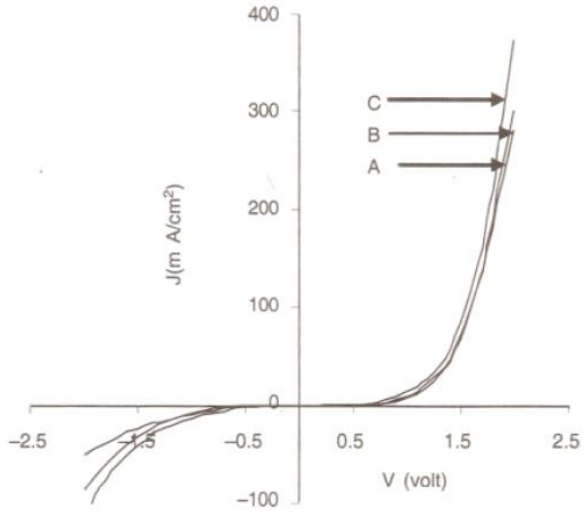

Figure 2. J-V characteristics of three ITO-(p)Si junctions of different cross-sectional area at room temperature in dark

the current increases slowly with voltage and did not show any tendency of saturation. The J-V characteristics followed the standard diode equation [11]

$$J = J_0 \exp(qV/nkT)\left[1 - \exp(-qV/kT)\right] \quad (1)$$

where, J is the current density of a diode for bias voltage V at temperature T (K), n is the diode ideality factor, J_0 is the saturation current density and other quantities has their usual meanings.

Figure 3 shows ln[J/{1-exp(-qV/kT)}] *vs* V plots for a few typical ITO-(p)Si junctions in dark at room temperature. At higher forward voltage (> 0.6V) the ln$J$-V plots of the junctions have been observed to deviate from linearity. This is due to presence of series resistance (R_s) associated with the neutral region of the diode. For this series resistance, the current of the diode is proportional to exp[$q(V\text{-}IR_s)/kT$ –1], instead of obeying the ideal condition [12]. At low voltage, the current is less, and hence the diode current can be characterized by equation (1). The ideality factor (n) calculated from the slopes and the saturation current density (J_0) calculated from the intercept of the linear region of the plots (Figure 3) for three junctions are tabulated in Table 1. The ideality factor have been found to be greater than the values reported earlier for this type of diode prepared by depositing ITO layer by other methods [2, 3]. However diode ideality factor can be affectively improved by controlling the deposition parameters which will be discussed later. The reverse current does not saturate and shows the tunneling probability due to lowering of potential barrier on application of bias.

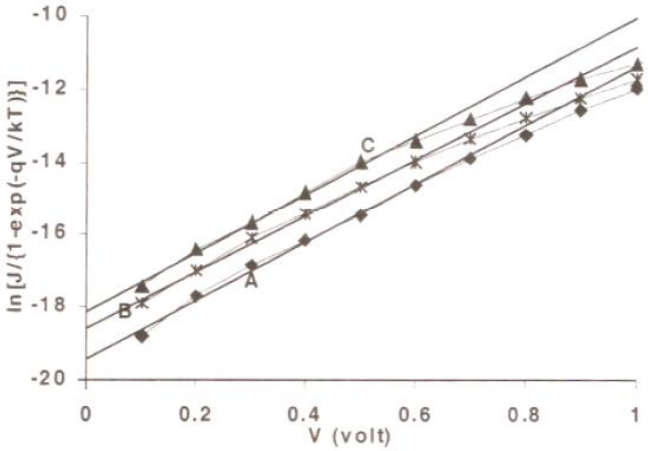

Figure 3. ln[J/{1–exp(–qV/kT)}] *vs* V curves of three ITO-(p)Si junctions at room temperature in dark.

Various factors were found to affect J-V characteristics and diode ideality factor in the present case. These curves depend on electrode area of the junctions. The existence of an interfacial layer of oxide on the surface of the silicon, image force lowering of the barrier heights, electron and hole recombination in the depletion region, tunneling effect

Table 1. Diode parameters of three typical ITO-(p)Si junctions at room temperature (303K).

Junction	Junction area (cm^2)	Ideality factor n	Saturation current density J_0(nA/cm^2)	Barrier height Φ(eV)	Series resistance R_s (KΩ)	Open circuit voltage (mV)	Short-circuit current density (mA/cm^2)	Fill factor
A	0.030	4.76	3	0.593	17	475	0.48	0.266
B	0.034	5.134	9	0.581	20	450	0.60	0.224
C	0.038	5.2	15	0.575	23	435	0.75	0.212

are the main reasons for the ideality factor (n) to be greater than unity. The effect of interfacial layer also contributed to high reverse current.

The series resistance estimated from ln$J$ *vs* V plots (not shown here) of the diodes are tabulated in Table1. In the present case, the large value of series resistance is contributed by the high sheet resistance of ITO layer and the resistance offered by the junction (interfacial oxide layer).

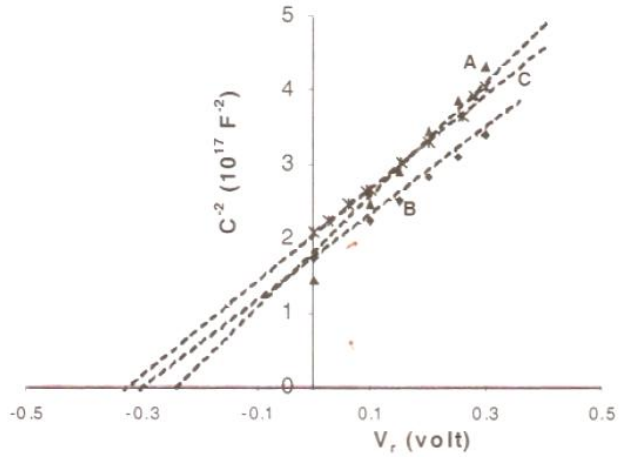

Figure 4. C^{-2} *vs* V(reverse) plots for three ITO-(p)Si junctions at room temperature in dark.

The C^{-2}–V plots for three junctions have been drawn at frequency 1KHz (Figure 4) for reverse bias. The carrier concentration and the built-in potential at the junction are estimated from the slope and intercept of C^{-2}–V plots of the junction under reverse bias condition using the following relation [13]

$$C^{-2} = \left(2(V_{bi} - V - kT/q) \Big/ q\varepsilon N_D \right). \tag{2}$$

Here V_{bi} is the built in potential at zero bias which is equal to V_i+kT/q, where V_i is the negative intercept on the V_r axis and ε is the permittivity of Si. The carrier concentration evaluated from the slopes is of the order of 10^{15} cm^{-3}. The barrier height is calculated from the measured value of V_{bi} from $\phi_b = qV_{bi} + (E_F - E_V)$, where $E_F - E_v$ is the difference between valence band energy and Fermi energy, and depends upon the doping density in the following way,

$$E_F - E_V = \frac{kT}{q} \ln\left(\frac{N_v}{N_a} \right) \tag{3}$$

where N_v is the effective density of states in valence band. The barrier height obtained for these junctions is nearer to 0.6 eV, which is less than the barrier height obtained by Vasu *et al* [2] by controlling the thickness of interfacial oxide layer.

The ITO-(p)Si junctions were studied for its photovoltaic performances. Figure 5 shows *J-V* curves of three typical junctions when illuminated by light of intensity 50 mW/cm^2. Nearly linear nature of the curves implies the existence of a large series resistance. Table 1 shows the open-circuit voltage, short-circuit current and fill-factor of a typical junction. Very low photovoltage (~450 mV) has been observed in the junctions due higher value diode ideality factor as reported by Mirzah *et al* [3]. The high defect density present with thermally evaporated ITO layer, presence of interfacial layer, presence of high series resistance and low conductivity of ITO layer are responsible for poor photovoltaic performance of the device.

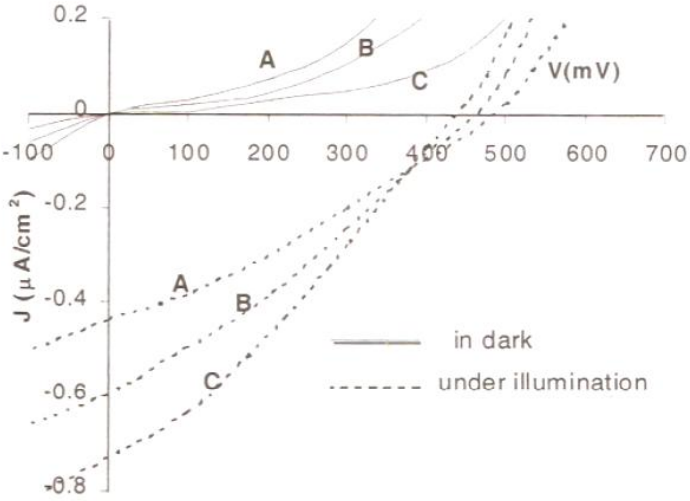

Figure 5. Photovoltaic effect of three typical ITO-(p)Si junctions under 50mW/cm^2 light intensity.

4. Conclusion

The study showed that rectifying ITO-(p)Si heterojunction diode can be fabricated by thermally depositing ITO films on silicon wafer. The diodes have high series resistance because of the low conductivity of thermally deposited ITO layer with high defect density and presence of interfacial layer. These causes are thought to affect the *J–V* characteristics as well as PV effect of the junctions. The recombination of photogenerated carriers at the interface states, low barrier height are also responsible for low photovoltaic performance. There are immense probabilities for improving the junction performance by controlling and optimizing the deposition parameters. The works are on progress to improve the diode quality and PV effect by controlling the deposition parameters of the ITO layer and post deposition annealing for suitable conductivity and transmittivity with an interfacial layer of optimum thickness.

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References

[1] H Kobayashi, T Ishida, Y Nakato and H Tsubomura *J. Appl. Phys.* **69** 1736 (1991)

[2] V Vasu and S Subrahmanyam *Semicond. Sci. Technol.* **7** 320 (1992)

[3] T Mizrah and D Adler *Appl. Phys. Lett.* **29** 682 (1976)

[4] J Touskova, J Kovanda, L Dobiasova, V Parizek and P Kielar *Sol. Energy Mater Sol Cell.* **37** 357 (1995)

[5] H L Ma, D H Zhang, P Ma, S Z Win and S Y Li *Thin Solid Films* **263** 105 (1995)

[6] A Salehi *Thin Solid Films* **324** 214 (1998)

[7] S Chaliha, M N Borah, P C Sarmah and A Rahman *Proc. of the 6th Asian Thermophysical Properties Conference* (Guwahati, India) 750 (2001)

[8] K L Chopra *Thin Film Phenomena* (New York : McGraw-Hill Company) 102 (1969)

[9] P C Sarmah and A Rahman *Bull. Mater. Sci.* **21** 149 (1998)

[10] S Chaliha, M N Borah, P C Sarmah and A Rahman *Proc. of the DAE Solid State Physics Symposium* (India) **50** 395 (2005)

[11] E H Rhoderik Metal Semiconductor Contacts (Oxford : Clarendon Press) 87 (1978)

[12] E H Rhoderik *Metal Semiconductor Contacts* (Oxford : Clarendon Press) 7 (1978)

[13] S M Sze *Physics of Semiconductor Devices* (2nd Edn) (New Delhi : Willey Eastern Ltd) 249 (1986)